

## IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A thin film transistor array substrate comprising:  
an insulating substrate;  
a first signal line formed on the insulating substrate;  
a first insulating layer formed on the first signal line;  
a second signal line formed on the first insulating layer while crossing over the  
first signal line;  
a thin film transistor connected to the first and the second signal lines;  
a second insulating layer formed on the thin film transistor, the second insulating  
layer having dielectric constant about 4.0 or less, the second insulating layer is formed  
with an a-Si:C:O layer or an a-Si:O:F layer and the second insulating layer having a first  
contact hole exposing a predetermined electrode of the thin film transistor; and  
a first pixel electrode formed on the second insulating layer while being connected  
to the predetermined electrode of the thin film transistor through the first contact hole.

2. (Original) The thin film transistor array substrate of claim 1, wherein the  
first insulating layer includes a top layer and a bottom layer, the bottom layer having  
dielectric constant about 4 or less, and the top layer being a silicon nitride layer.

3-6. (Canceled)

7. (Previously presented) The thin film transistor array substrate of claim 1,  
wherein the a-Si:C:O layer is formed through plasma enhanced chemical vapor deposition  
(PECVD) using a gaseous material selected from the group consisting of SiH(CH<sub>3</sub>)<sub>3</sub>,  
SiO<sub>2</sub>(CH<sub>3</sub>)<sub>4</sub>, (SiH)<sub>4</sub>O<sub>4</sub>(CH<sub>3</sub>)<sub>4</sub>, and Si(C<sub>2</sub>H<sub>5</sub>O)<sub>4</sub> and an oxide agent of N<sub>2</sub>O or O<sub>2</sub>.

8. (Previously presented) The thin film transistor array substrate of claim 1, wherein the a-Si:O:F layer is formed through plasma enhanced chemical vapor deposition (PECVD) by introducing a material selected from the group consisting of SiH<sub>4</sub> and SiF<sub>4</sub> with CF<sub>4</sub> and O<sub>2</sub> added.

9. (Original) The thin film transistor array substrate of claim 1, wherein the second insulating layer has a dielectric constant of about 2 to about 4.

10. (Original) The thin film transistor array substrate of claim 1, wherein the first signal line includes a first alloy layer and a second alloy layer, the first alloy layer is a Cr alloy layer or a Mo alloy layer and the second alloy layer is a Al alloy layer or a Ag alloy layer.

11. (Original) The thin film transistor array substrate of claim 1, wherein the first pixel electrode is made of an optically transparent and electrically conductive material.

12. (Original) The thin film transistor array substrate of claim 11, wherein the transparent conductive material is indium tin oxide (ITO) or indium zinc oxide (IZO).

13-32. (Canceled)

33. (Currently Amended) A thin film transistor array substrate comprising:  
an insulating substrate;  
a first signal line formed on the insulating substrate;  
a first insulating layer formed on the first signal line;  
a second signal line formed on the first insulating layer while crossing over the first signal line;  
a thin film transistor connected to the first and the second signal lines;

a second insulating layer formed on the thin film transistor, the second insulating layer having dielectric constant about 4.0 or less, and the second insulating layer having a first contact hole exposing a predetermined electrode of the thin film transistor; and

a first pixel electrode formed on the second insulating layer while being connected to the predetermined electrode of the thin film transistor through the first contact hole,

wherein the first insulating layer includes a top layer and a bottom layer, the bottom layer being an a-Si:O:F layer having dielectric constant about 4 or less, and the top layer being a silicon nitride layer.

34. (Canceled)

35. (Previously Presented) The thin film transistor array substrate of claim 34, wherein the a-Si:C:O layer is formed through plasma enhanced chemical vapor deposition (PECVD) using a gaseous material selected from the group consisting of SiH(CH<sub>3</sub>)<sub>3</sub>, SiO<sub>2</sub>(CH<sub>3</sub>)<sub>4</sub>, (SiH)<sub>4</sub>O<sub>4</sub>(CH<sub>3</sub>)<sub>4</sub>, and Si(C<sub>2</sub>H<sub>5</sub>O)<sub>4</sub> and an oxide agent of N<sub>2</sub>O or O<sub>2</sub>.

36. (Previously Presented) The thin film transistor array substrate of claim 34, wherein the a-Si:O:F layer is formed through plasma enhanced chemical vapor deposition (PECVD) by introducing a material selected from the group consisting of SiH<sub>4</sub> and SiF<sub>4</sub> with CF<sub>4</sub> and O<sub>2</sub> added.

37. (Previously Presented) The thin film transistor array substrate of claim 33, wherein the second insulating layer has a dielectric constant of about 2 to about 4.

38. (Previously Presented) The thin film transistor array substrate of claim 33, wherein the first signal line includes a first alloy layer and a second alloy layer, the first alloy layer is a Cr alloy layer or a Mo alloy layer and the second alloy layer is a Al alloy layer or a Ag alloy layer.

39. (Previously Presented) The thin film transistor array substrate of claim 33, wherein the first pixel electrode is made of an optically transparent and electrically conductive material.

40. (Previously Presented) The thin film transistor array substrate of claim 39, wherein the transparent conductive material is indium tin oxide (ITO) or indium zinc oxide (IZO).

41-56. (Withdrawn)